AMENDMENTS TO THE SPECIFICATION

The following is a marked up version of each replacement paragraph and/or section of the specification in which underlines indicates insertions and strikethrough indicates deletions.

Please replace the paragraph on page 4, lines 8-9 with the following paragraph:

~~Fig.~~ Figs. ~~1 illustrates~~ 1A and 1B illustrate a buried fuse reading device according to an embodiment of the present invention; and

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Please replace the paragraph on page 4, lines 12-16 with the following paragraph:

Fig. ~~1~~ 1A illustrates a buried fuse reading device according to an embodiment of the present invention. As shown, the buried fuse reading device includes a bias generator 10 supplying first and second bias voltages on first and second bias voltage lines BHI and BLO to a sense amplifier 50 and a validation circuit 70.

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Please replace the paragraph on page 5, lines 15-28 with the following paragraph:

The sense amplifier 50 includes a second PMOS transistor 54 and a third NMOS transistor 56 connected in series with a fuse 52 between the high voltage line VDD and the low voltage line VSS. In a preferred embodiment, the fuse 52 is a buried metal fuse. The sources of the second PMOS transistor 54 and the third NMOS transistor 56 are connected at a node FUSEN to an inverter 58. The output of the inverter 58 serving as the output OUT of the buried fuse reading circuit. While only one fuse and sense amplifier has been illustrated in Fig. ~~1~~ 1A for the sake of clarity, it will be understood by those skilled in the art that numerous fuses and sense amplifiers (e.g., 15 other fuses and sense amplifiers) could be connected in parallel with the illustrated sense amplifier 50 and fuse 52 as shown in Fig. 1B. Fig. 1B is the same as Fig. 1A except that the sense amplifier 50 and fuse 52 are shown as being parallel. The number of parallel instances of sense

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amplifier 50 and fuse 52 may be from 1 to n; where n is the total number of parallel instances. As further shown in Fig. ~~1~~ 1A, the gates of the second PMOS transistor 54 and the third NMOS transistor 56 are connected to the first and second bias voltage lines BHI and BLO, respectively.

Please replace the paragraph on page 6, lines 1-11 with the following paragraph:

Continuing to refer to Fig. ~~1~~ 1A, the validation circuit 70 includes a third PMOS transistor 72 and a fourth NMOS transistor 74 connected in series between the high voltage line VDD and the low voltage line VSS. The third PMOS transistor 72 and the fourth NMOS transistor 74 are weaker (i.e., have a smaller drive capability) than the second PMOS transistor 54 and the third NMOS transistor 56, respectively. An inverter 76 is connected to the sources of the third PMOS transistor 72 and the fourth NMOS transistor 74 at a node VALID, and the output of the inverter 76 produces the INVALID output of the validation circuit 70.

Please replace the paragraph on page 6, lines 10-21 with the following paragraph:

Next the operation of the buried fuse reading circuit illustrated in Fig. ~~1~~ 1A will be described with reference to Fig. ~~1~~ 1A and Figs. 2A-2G. Figs. 2A-2G illustrate signals input and output from elements in the buried fuse reading circuit. When the buried fuse reading circuit is in a powered down state, the control signal PDN is low as shown in Fig. 2A. In this state, the first, second and fourth power control transistors 20, 22 and 26 are off and do not conduct. However, the third and fifth power control transistors 24 and 28 are turned on and do conduct. As such, the first bias voltage line BHI is pre-charged up to the high voltage on the high voltage line VDD via the third power control transistor 24 as shown in Fig. 2B, and the second bias voltage line BLO is also pre-charged up to the high voltage on the high voltage line VDD via the third and fifth power control transistors 24 and 28 as shown in Fig. 2C.